REMARKS

Applicant is reminded of the proper language and format for an abstract of the disclosure. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Ueno (Japanese Patent Publication 01-107527). Claims 1-2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno as applied to claim 3 above, and further in view of Adair (US Patent 6,184,151).

1. Objection of the disclosure:

The abstract of the disclosure is objected to because it has more than 150 words. Correction is required.

Response:

The abstract of the disclosure is amended as shown in the "Amendment" section. Reconsideration of the corrected disclosure is hereby requested.

2. Rejection of claim 3 under 35 U.S.C. 102(b):

Ueno teaches a method of preventing two-dimensional (optical proximity) effects caused by light diffraction during a photolithography process to form (define) a rectangular (array) pattern. A negative photosensitive resin (photoresist) is formed on a semiconductor substrate. The photoresist is exposed through a first linear mask pattern, 100 (having parallel lines, 101), shown in Figure 1(a). Then the photoresist is exposed through a second linear mask pattern, 200 (having parallel lines, 201), shown in Figure 1(b) and positioned in perpendicular relation to the first exposure pattern to form an array of rectangular unexposed photoresist regions, 400, shown in Figure 2(a).

Response:

Claim 3 has been canceled as shown in the "Amendment" section.

3. Rejection of claim 1-2 and 4-6 under 35 U.S.C. 103(a):

Ueno is discussed above, but does not specify subsequent etching of the substrate using the remaining photoresist pattern as an etching mask and does not specify the formation of storage nodes for a dynamic random access memory (DRAM). Ueno also does not specify that the optical proximity effect to be avoided were corner rounding and pattern shortening.

Adair states that in order to scale down DRAM devices while maintaining sufficient capacitance, corner rounding and shortening effects should be avoided when forming the storage nodes (capacitors) in column 1, at lines 46-53. Adair also teaches plural perpendicular exposures (using masks having parallel linear patterns) of one or more photoresist layers to obtain sharp-edged corners (without significant corner rounding or image shortening) in the resulting photoresist image, followed by etching of an underlying substrate through the remaining photoresist pattern as an etching mask in column 6, at lines 6-50.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the Ueno double exposure method to form a rectangular array of unexposed photoresist portions with the DRAM storage node formation by subsequent etching taught by Adair. The expected result of this combination would be to avoid corner rounding and image shortening during DRAM storage node formation.

Response:

The applicant's invention provides a method of forming storage nodes in a DRAM on a semiconductor wafer. The method

comprises performing a first exposure process to form **first exposure regions including a plurality of lines parallel to each other and covering each storage node**, and performing a second exposure process to form **second exposure regions cutting the plurality of lines of the first exposure regions**. The first exposure regions and the second exposure regions of the photoresist layer are then removed for forming an array photoresist layer on a thin film layer positioned on the semiconductor wafer. The array photoresist layer functions as a mask to perform an etching process to the thin film layer for forming an array thin film layer as a storage nodes in the DRAM. It is an advantage of the applicant's invention that **a first exposure process is performed to form linear and parallel first exposure regions followed by performing a second exposure process to form interlaced second exposure regions for defining the position of the storage nodes, and optical proximity effects are decreased.**

Ueno (Japanese Patent Publication 01-107527) provides forming method for pattern and eliminating two-dimensional effect due to the diffracting of a light. As shown in the figures, the method uses two photomasks for forming a rectangular pattern, and **the rectangular pattern is defined by crossing parts of the linear mask patterns of the two photomasks.**

Adair (US 6,184,151) provides a method for forming images having sharp corners during lithographic processing and a photomask formed thereby. As shown in Fig.4, the method first forms a blocking layer 120, a hard mask 130 and a photoresist layer 140 on a substrate 112. Then as shown in Fig.5, the method comprises defining patterns of the photoresist layer 140 and forming a plurality of parallel lines in the hard mask 130.

Another photoresist layer 150 is formed on the substrate 112, as shown in Fig.7, a plurality of line patterns perpendicular to the lines of the hard mask 130 are defined in the photoresist layer 150. Finally, an etching process is performed to remove the blocking layer 120 not covered by the phtoresist layer 150 and the hard mask 130 for exposing portions of the substrate 112. As shown in Fig.9, **because the substrate 112 is made from a transparent material and the exposed portions of the substrate are rectangular regions, sharp corner images can be formed by using the exposed portions of the substrate during a photolithographic process.**

The combination of Ueno's invention and Adair's invention discloses a double exposure method to form a rectangular array of unexposed photoresist portions with the DRAM storage node formation by subsequent etching process, however, **the rectangular array of unexposed photoresist is defined by crossing parts of the linear mask patterns of two photomasks** used in the double exposure method. Consequently, like applicant's admitted prior art, portions of the photoresist layer are exposed twice, forming a plurality of overexposure areas that causes more severe optical proximity effects.

Comparatively, the applicant's invention method performs a first exposure process to form first exposure regions including a plurality of lines parallel to each other and performs a second exposure process to form second exposure regions **cutting the plurality of lines of the first exposure regions so as to define the rectangular array of unexposed photoresist.** Therefore, no overexposure areas are formed due to twice exposure.

In view of the foregoing, applicant believes that the limitations of claims 1-2 of the applicant's invention are different from the Ueno and Adair. The applicant has canceled claims 3-6 and amended claims 1 for overcoming the rejection, and no new matter is included. Reconsideration of claims 1-2 is politely requested.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Abstract:

On page 1, please replace the whole paragraph beginning on line 4 as following:

A dynamic random access memory (DRAM) is formed on a semiconductor wafer including a substrate, a thin film layer positioned on the substrate, and a photoresist layer positioned on the thin film layer. A first exposure process is performed to form first exposure regions including a plurality of lines parallel to each other and covering each storage node. A second exposure process is performed to form second exposure regions cutting the plurality of lines of the first exposure regions. The first exposure regions and the second exposure regions of the photoresist layer are then removed for forming an array photoresist layer on the thin film layer. The array photoresist layer functions as a mask to perform an etching process to the thin film layer for forming an array thin film layer as a storage nodes in the DRAM.

In the claim:

1. (Once Amended) A method of forming storage nodes in a dynamic random access memory (DRAM) on a semiconductor wafer, the semiconductor wafer comprising a substrate, a thin film layer positioned on the substrate, and a photoresist layer positioned on the thin film layer, the method comprising:

performing a first exposure process to form first exposure regions [that are linear and parallel with each other on the photoresist layer] including a plurality of lines that are parallel to each other and covering each storage node;

performing a second exposure process to form second exposure regions [that are interlaced with and perpendicular to each other on the photoresist layer] cutting the plurality of lines of the

first exposure regions;

performing a development process on the first exposure regions and the second exposure regions of the photoresist layer;

removing the first exposure regions and the second exposure regions of the photoresist layer to form an array photoresist layer on the thin film layer; and

using the array photoresist layer as a mask to perform an etching process to remove portions of the thin film layer not covered by the array photoresist layer so as to form an array thin film layer, the array thin film layer being used as the storage nodes in the DRAM.

Cancel claims 3-6.

Sincerely yours,

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